

DOCKET NO. NL010554
 SERIAL NO. 10/073,706
 PATENT

REMARKS

Claims 1-11 are pending in the application. All claims were rejected. A Notice of Appeal is filed concurrently with this Response.

35 U.S.C. § 112(1) – Enablement

Claims 7-8 were rejected as non-enabled by the specification. The Examiner reads the limitations of these claims as shown in Figures 5 and 6, each described in paragraphs 0030 and 0031, respectively, as an “all-pass network,” as implementations of the “all-pass circuit” element 10 of Figure 4 is described.

Claims 7 and 8 describe different structural implementations of the “splitting means” of Claim 1.

Figure 5 shows input signal i_i , which is mirrored to phase-shifted output i_o . The skilled artisan recognizes that Figure 5's i_i corresponds to Figure 4's i_{in} , and Figure 5's i_i and i_o correspond to Figure 4's i_1 and i_2 , respectively. The transfer function of the circuit of Figure 5 is $\frac{i_o}{i_i} = \frac{sC/g_m - 1}{sC/g_m + 1}$, so that the time constant can be tuned by adjusting I_{BIAS} .

With regard to Figure 6, applicant first notes that the application specifically describes that the inputs to the circuit can be either voltages or currents (see, e.g., paragraph 0036), and Claim 1 does not specifically require either, so the Examiner's observation that the circuit of Figure 6 receives input voltages does not appear to be relevant. Paragraph 0048 describes that the input voltage is converted into current, and following paragraphs describe this circuit as producing current i_A and corresponding phase-shifted current i_B at the output.

One of skill in the art understands that the circuits shown in both Figures 5 and 6 receive

DOCKET NO. NL010554
SERIAL NO. 10/073,706
PATENT

an input signal and produce corresponding phase-shifted output signals, as does element 10 in Figure 4.

Figures 5 and 6, and claims 7 and 8, are therefore believed to be fully enabled, and these rejections are traversed.

35 U.S.C. § 112(2) – Definiteness

The Office Action presents a new indefiniteness rejection with regard to Claims 7 and 8, discussed above. Initially, the Applicant notes that the Examiner appears to be unclear as to whether these claims relate to the “splitting means” of Claim 1; it is respectfully suggested that these claims, as amended in the previous Amendment, are very clearly drawn to the “splitting means.”

The interrelation of the splitting means with the other elements of Claim 1 is believed to be clear in that claim. Claims 7 and 8 specify the structure of alternate embodiments of the “splitting means,” and it is believed that the structure described is sufficient to particularly point out and distinctly claim the particular structures. Indeed, it is hard to imagine that one of skill in the art would not immediately understand the interrelation of all elements described in each of these claims.

DOCKET NO. NL010554
SERIAL NO. 10/073,706
PATENT

All §112(2) rejections are traversed. However, if the Examiner has a specific concern or suggestion as to how these claims may be made even more clear, he is respectfully invited to telephone the undersigned attorney.

35 U.S.C. § 101 – Double Patenting

The Examiner's provisional double patenting rejection has been noted. As this is a provisional rejection only, it need not be addressed until this application or co-pending application 10/217,825 is issued.

35 U.S.C. § 102 – Anticipation

Claims 1-6 and 11 have been rejected as anticipated by Ishihara (USP 6,054,883). The Examiner correctly notes that some elements of Ishihara appear to be similar to elements of claim 1. Claim 1, and amended claim 11, require that the splitting means also have the characteristics of an "all-pass," which the specification describes as a circuit that "produces two quadrature signals with equal amplitudes and the gm/C time constant of an all-pass tracks the oscillation frequency (using the same tuning mechanism) of the input signal outputted by the oscillator".

Nothing in Ishihara appears to teach or suggest this feature. The Examiner indicates that he does not find the description cited above to be a "definition," and indicates that this description cannot be read into the claims from the specification.

The Office Action appears to ignore the broader issue that claims 1 and 11 specifically claim that the splitting means have the characteristics of an all-pass, and this feature – wh ther

DOCKET NO. NL010554
SERIAL NO. 10/073,706
PATENT

"all-pass" is taken as described in the specification or by some other definition – is not taught or suggested at all by Ishihara. If the Examiner believes this feature is present in Ishihara, he is respectfully requested to specifically point it out.

As an anticipation reference must teach EVERY aspect of the claims, and Ishihara does not, Ishihara fails to anticipate claims 1-6 and 11.

The anticipation rejections are traversed.

35 U.S.C. § 103(a) – Obviousness

Claims 7, 9, and 10 were rejected as obvious over Ishihara in view of Liu (USP 6,496,545). Applicant notes that no proper motivation to combine the Ishihara and Liu references has been stated. While both Ishihara and Liu incorporate phase shifters, Liu is directed toward a side-band mixer, and there is no indication that one designing a phase shifter, or even a phase shifter with error detection, would look to a side-band mixer patent for any teachings, nor that Ishihara is at all concerned with sideband rejection.

Moreover, although Liu's Figure 5A does indeed include two transistors and a capacitor, they are not connected to each other (or to themselves) as described in claim 7. As such, even this combination of references fails to meet the claim limitations.

Therefore, a *prima facie* obviousness rejection has not been made, and all obviousness rejections are traversed.

All rejections stated in the Office Action mailed 11/26/03 have been traversed.

DOCKET No. NL010554
SERIAL No. 10/073,706
PATENT

SUMMARY

For the reasons given above, the Applicants respectfully request reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@davismunck.com*.

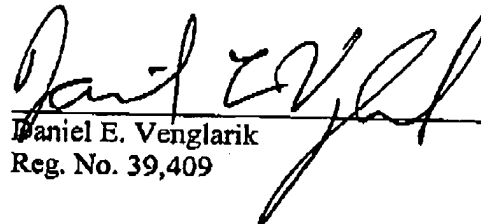
The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 1-6-04

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *dvenglarik@davismunck.com*


Daniel E. Venglarik
Reg. No. 39,409